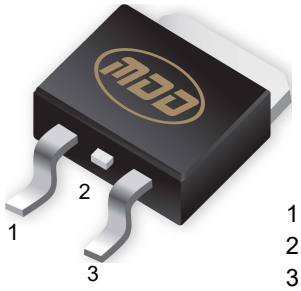
MDD80N03D

30V N-Channel Enhancement Mode MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$Max	I_D Max
30V	6mΩ@10V	80A
	9mΩ@4.5V	

TO-252



1. Gate
2. Drain
3. Source

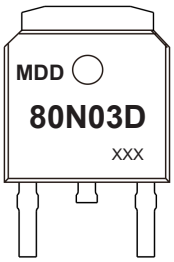
Features

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Halogen Free

Application

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

Marking



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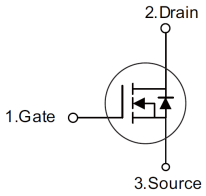
Equivalent Circuit



Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	80	A
Pulsed Drain Current (Note 1)	I_{DM}	190	A
Avalanche Energy Single Pulsed (Note 2)	E_{AS}	132	mJ
Power Dissipation	P_D	44	W
Thermal Resistance Junction-to-Case(Note 3)	$R_{\theta JC}$	2.8	℃/ W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{stg}	-50 ~+150	℃

Notes: 1.Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
2.Tj=25℃, VDD=25V, VG=10V, L=0.5mH, IAS=23A
3.$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Ta = 25℃ unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30	--	--	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=30V, V_{GS}=0V	--	--	1	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=20A	--	3.8	6	mΩ
		V_{GS}=4.5V, I_D=15A	--	4.8	9	mΩ

Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	V_{DS}=15V V_{GS}=0V f=1MHz	--	2504	--	pF
C_{oss}	Output Capacitance		--	323	--	pF
C_{rss}	Reverse Transfer Capacitance		--	283	--	pF
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=20A (Note1,2)	--	54	--	nC
Q_{gs}	Gate Source Charge		--	8.5	--	nC
Q_{gd}	Gate Drain Charge		--	10.2	--	nC

Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d(on)}$	Turn on Delay Time	V_{DS}=20V, V_{GS} =10V, I_D=2A, R_G=3Ω (Note1,2)	--	11.4	--	ns
t_r	Turn on Rise Time		--	20.4	--	ns
$t_{d(off)}$	Turn Off Delay Time		--	41	--	ns
t_f	Turn Off Fall Time		--	25	--	ns

Source Drain Diode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{SD}	Source drain current(Body Diode)		--	--	80	A
I_{SM}	Pulsed Current		--	--	190	A
V_{SD}	Drain-Source Diode Forward Voltage	I_S=20A, V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, V_{GS}=0V, dI/dt=100A/μs	--	15.1	--	ns
Q_{rr}	Body Diode Reverse Recovery Charge		--	6.5	--	nC

Notes: 1.Pulse test ; Pulse width 300us, duty cycle 2%.
2.Essentially independent of operating temperature.

■ Typical Performance Characteristics

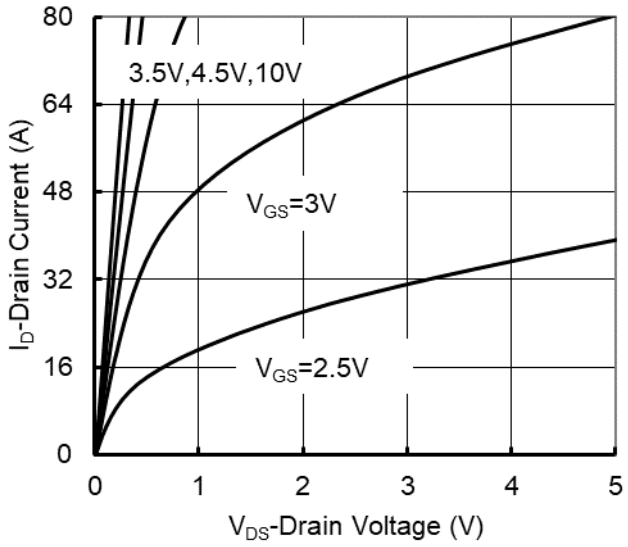


Figure 1. Output Characteristics

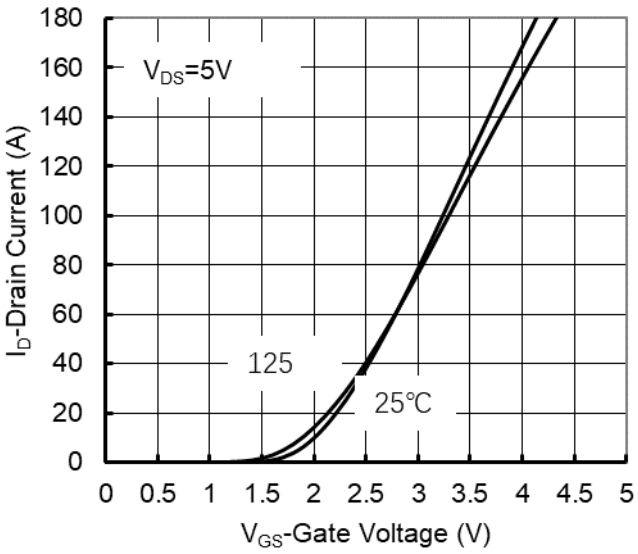


Figure 2. Transfer Characteristics

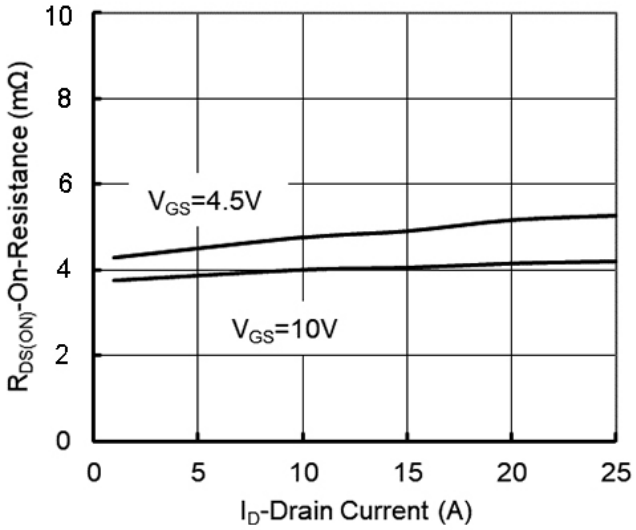


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

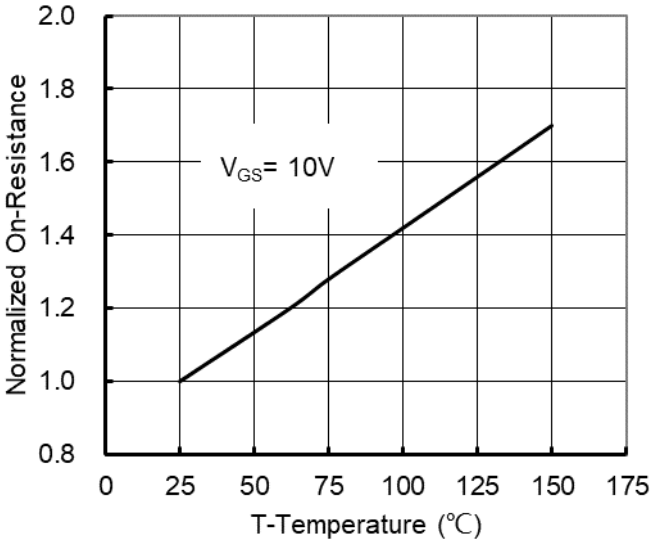


Figure 4. On-Resistance vs. Junction Temperature

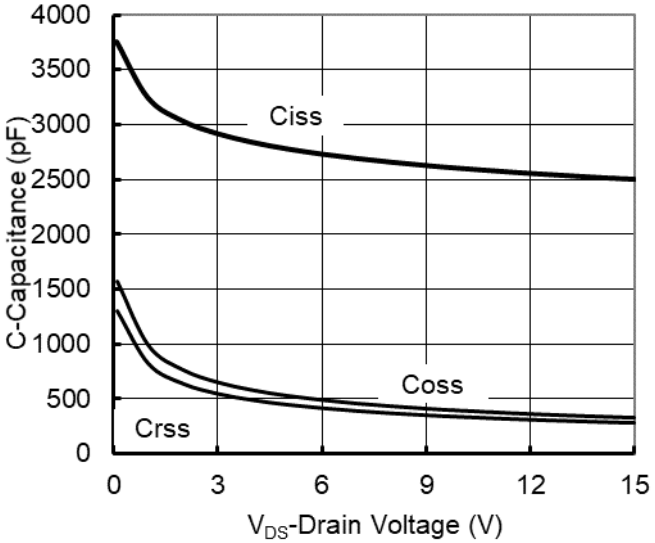


Figure 5. Capacitance Characteristics

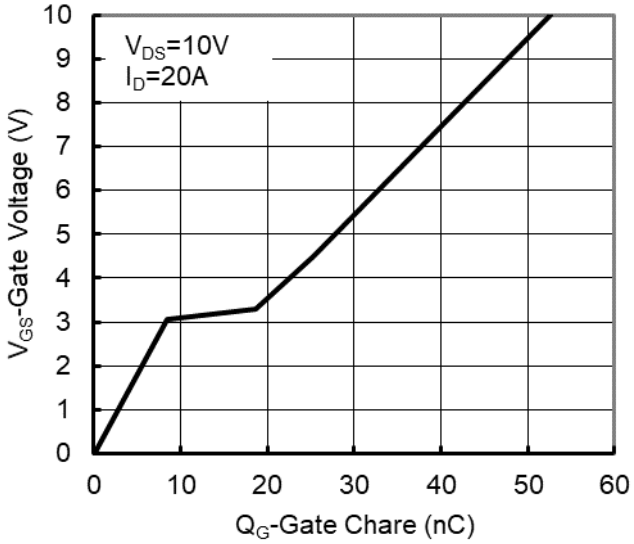


Figure 6. Gate Charge

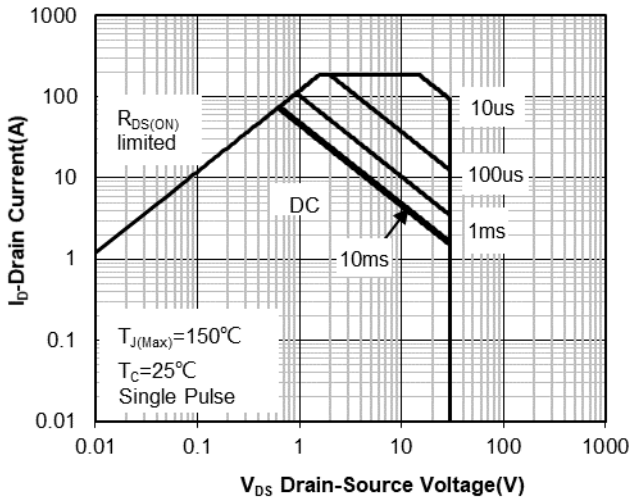


Figure 7. Safe Operation Area

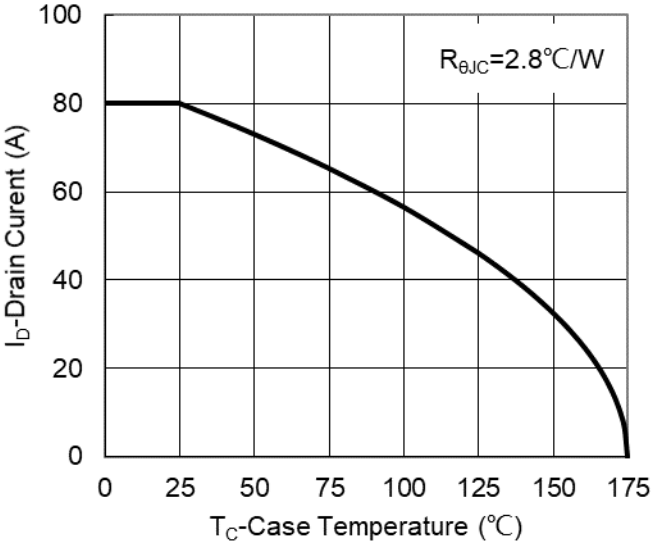


Figure 8. Maximum Continuous Drain Current vs Case Temperature

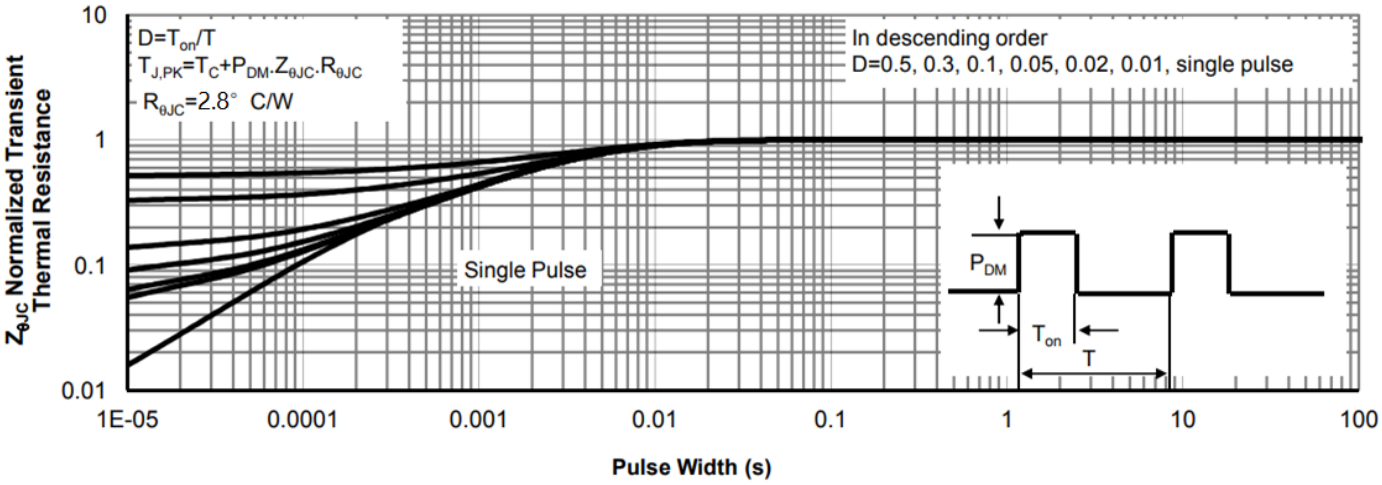
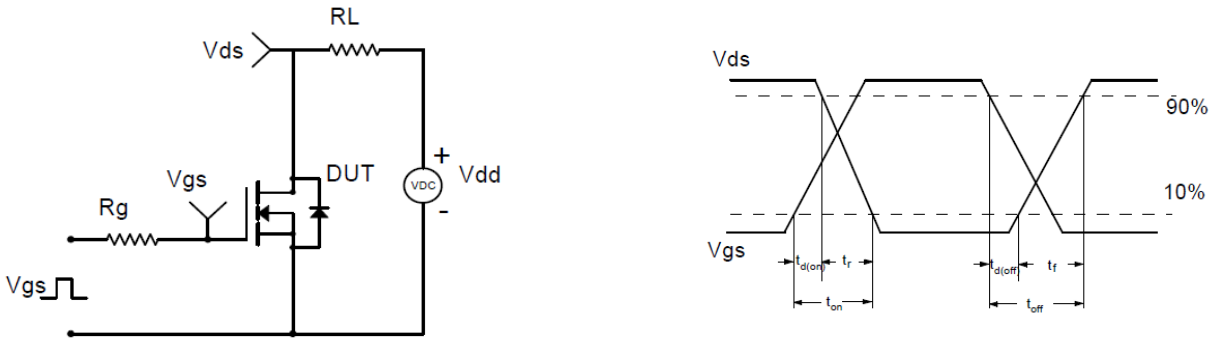
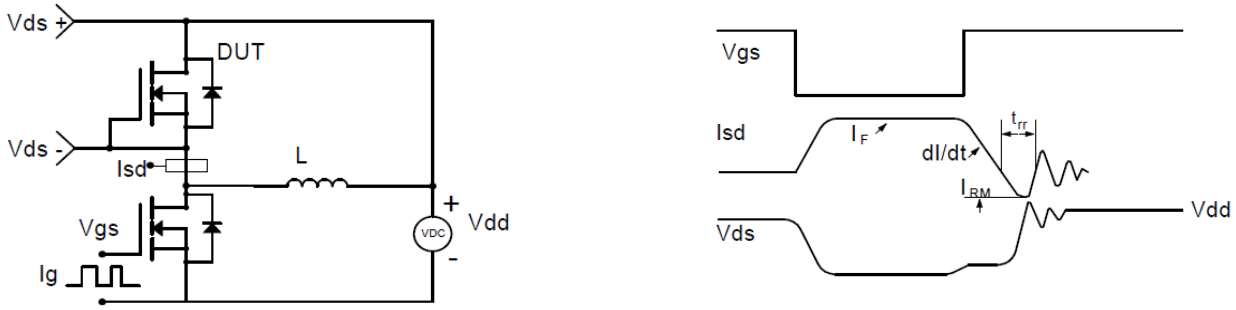


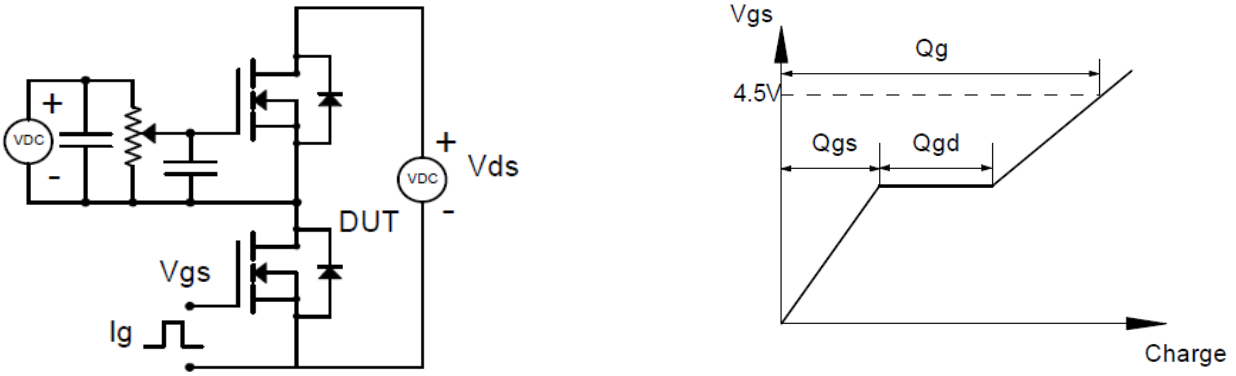
Figure 9. Normalized Maximum Transient Thermal Impedance



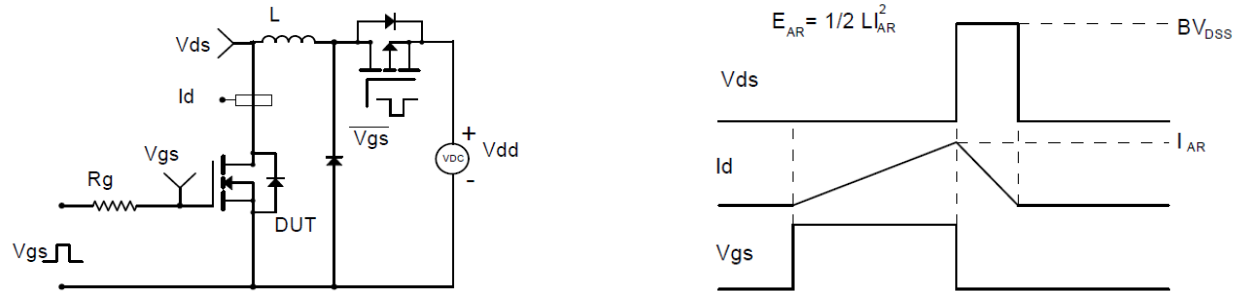
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



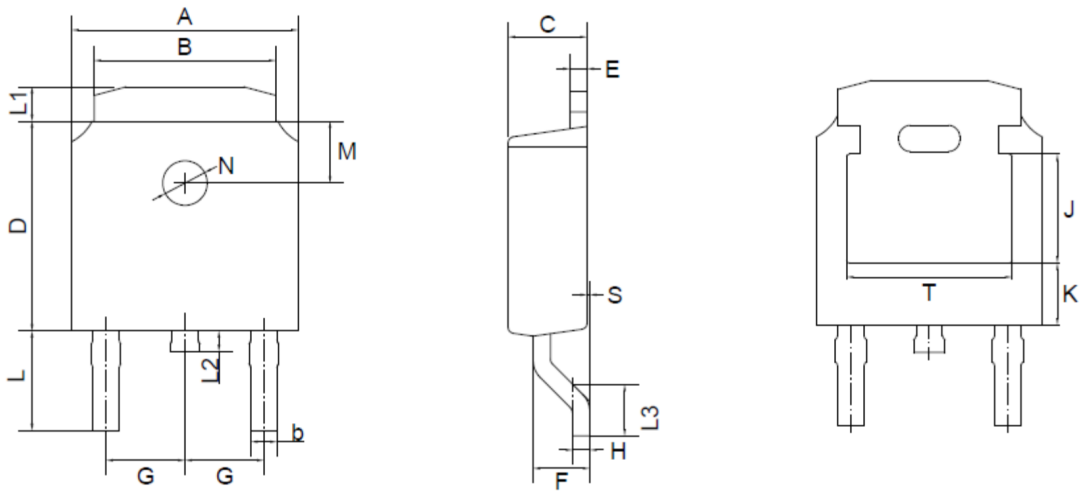
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Outlitne Drawing

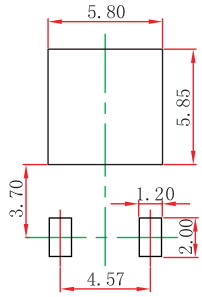
TO-252 Package Outline Dimensions



TO-252(D-PAK) mechanical data

UNIT		A	B	b	C	D	E	F	G	H	L	L1	L2	L3	S	M	N	J	K	T
mm	max	6.7	5.5	0.8	2.5	6.3	0.6	1.8	2.29 TYPICAL	0.55	3.1	1.2	1.0	1.75	0.1	1.8 TYPICAL	1.3 TYPICAL	3.16 ref.	1.80 ref.	4.83 ref.
	min	6.3	5.1	0.3	2.1	5.9	0.4	1.3		0.45	2.7	0.8	0.6	1.40	0.0					
mil	max	264	217	31	98	248	24	71	90 TYPICAL	22	122	47	39	69	4	71 TYPICAL	51 TYPICAL	124 ref.	71 ref.	190 ref.
	min	248	201	12	83	232	16	51		18	106	31	24	55	0					

Suggested Pad Layout



Note:
1.Controlling dimension:in/millimeters.
2.General tolerance: ±0.05mm.
3.The pad layout is for reference purposes only.