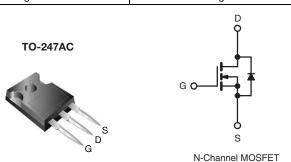


Power MOSFET

PRODUCT SUMMARY						
V _{DS} (V) at T _J max.	56	560				
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.270				
Q _g (Max.) (nC)	76					
Q _{gs} (nC)	21	21				
Q _{gd} (nC)	34					
Configuration	Single					



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Figure-of-Merit Ron x Qq
- 100 % Avalanche Tested
- High Peak Current Capability
- dV/dt Ruggedness
- Improved T_{rr}/Q_{rr}
- Improved Gate Charge
- High Power Dissipations Capability
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION			
Package	TO-247AC		
Lead (Pb)-free	SiHG20N50C-E3		
Lead (Pb)-free and Halogen-free	SiHG20N50C-GE3		

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	500	V	
Gate-Source Voltage			V_{GS}	± 30	V	
Continuous Prain Current (T. – 150 °C\8	V _{GS} at 10 V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$,	20		
Continuous Drain Current (T _J = 150 °C) ^e	V _{GS} at 10 V	T _C = 100 °C	I _D	11	Α	
Pulsed Drain Current ^a			I _{DM}	80		
Linear Derating Factor				1.8	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	361	mJ	
Maximum Power Dissipation			P_{D}	250	W	
Peak Diode Recovery dV/dtc			dV/dt	5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	- °C	
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d]	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 2.5 mH, $R_g = 25$ Ω , $I_{AS} = 17$ A.
- c. $I_{SD} \le 18$ A, $dI/dt \le 380$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- d. 1.6 mm from case.
- e. Limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	40	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.5]	

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1				•	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0 V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	700	-	mV/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} :	= V _{GS} , I _D = 250 μA	3.0	=-	5.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 30 V	-	=-	± 100	nA
Zon Oale Wellers Buris O mad		V _{DS} :	= 500 V, V _{GS} = 0 V	-	-	25	μА
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 \	/, V _{GS} = 0 V, T _J = 125 °C	-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A	-	0.225	0.270	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 50 V, I _D = 10 A	-	6.4	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}$		-	2451	2942	_
Output Capacitance	C _{oss}			-	300	360	pF
Reverse Transfer Capacitance	C_{rss}			-	26	32	
Total Gate Charge	Qg			-	65	76	
Gate-Source Charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$V_{GS} = 10 \text{ V}$ $I_D = 18 \text{ A}, V_{DS} = 400 \text{ V}$		21	-	nC
Gate-Drain Charge	Q_{gd}				29	-	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 250 V, I_{D} = 18 A, R_{g} = 9.1 Ω		-	80	-	ns
Rise Time	t _r			ı	27	-	
Turn-Off Delay Time	$t_{d(off)}$			ı	32	-	
Fall Time	t _f			ı	44	-	
Gate Input Resistance	R_{g}	f = 1 MHz, open drain		-	1.1	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	
Pulsed Diode Forward Current	I _{SM}			-	-	80	- A
Body Diode Voltage	V_{SD}	T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dl/dt = 100 A/µs, V = 35 V		-	503	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	6.7	-	μC
Reverse Recovery Current	I _{RRM}			-	30	-	Α

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

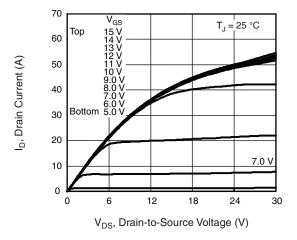


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

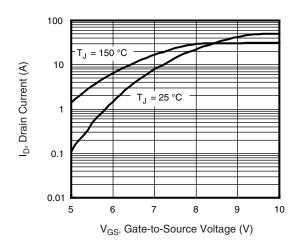


Fig. 3 - Typical Transfer Characteristics

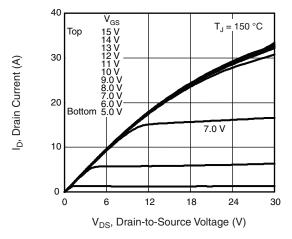


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

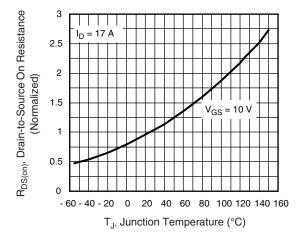


Fig. 4 - Normalized On-Resistance vs. Temperature



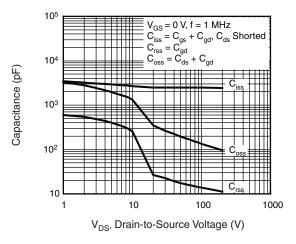


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

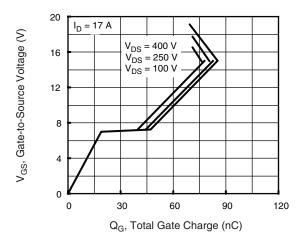


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

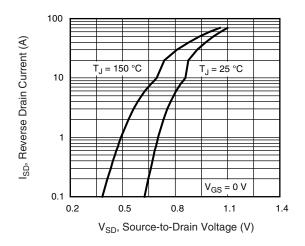


Fig. 7 - Typical Source-Drain Diode Forward Voltage

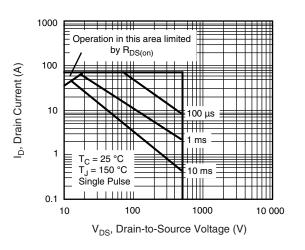


Fig. 8 - Maximum Safe Operating Area

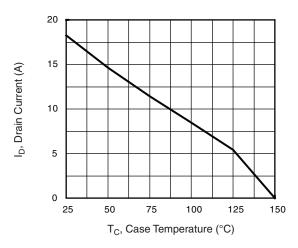


Fig. 9 - Maximum Drain Current vs. Case Temperature



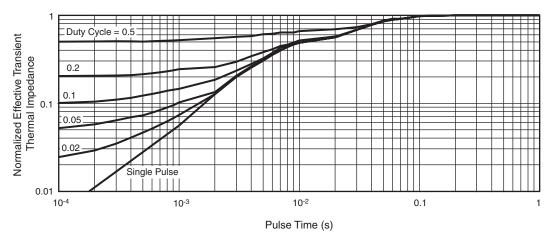


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (TO-247)

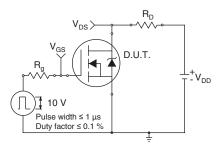


Fig. 11a - Switching Time Test Circuit

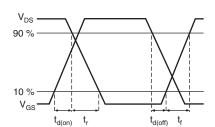


Fig. 11b - Switching Time Waveforms

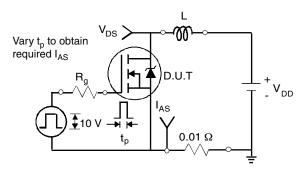


Fig. 12a - Unclamped Inductive Test Circuit

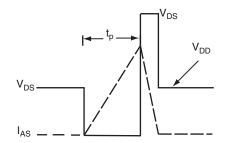


Fig. 12b - Unclamped Inductive Waveforms

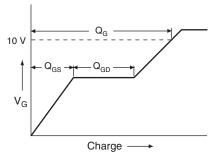


Fig. 13a - Basic Gate Charge Waveform

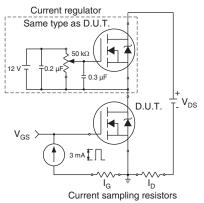
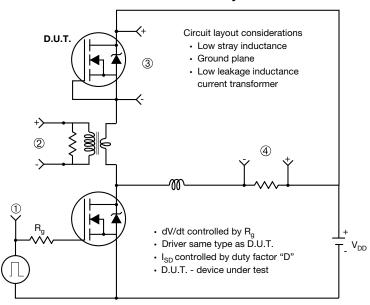


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



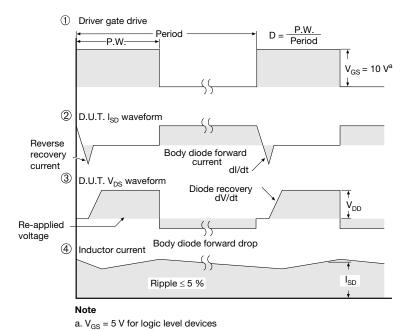


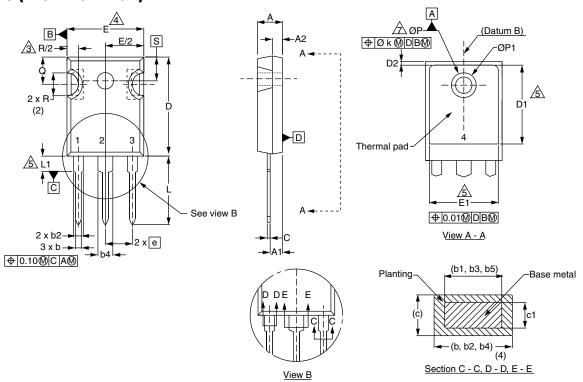
Fig. 14 - For N-Channel

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TO-247AC (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.65	5.31	0.183	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.65	2.39	0.065	0.094
b3	1.65	2.37	0.065	0.093
b4	2.59	3.43	0.102	0.135
b5	2.59	3.38	0.102	0.133
С	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.70	0.776	0.815
D1	13.08	-	0.515	-

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
Е	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
е	5.46	BSC	0.215 BSC	
Øk	0.254		0.010	
L	14.20	16.10	0.559	0.634
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ØΡ	3.56	3.66	0.140	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: S-81920-Rev. A, 15-Sep-08 DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

- 2. Contour of slot optional.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions D1 and E1.
- 5. Lead finish uncontrolled in L1.
- 6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- 7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.

Document Number: 91360
Revision: 15-Sep-08
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